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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,569	06/15/2005	Edwin Rijpkema	NL021331	9459
65913	7550	09/23/2008	EXAMINER	
NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			MITCHELL, DANIEL D	
			ART UNIT	PAPER NUMBER
			2619	
			NOTIFICATION DATE	DELIVERY MODE
			09/23/2008	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

### Office Action Summary

**Application No.**

10/538,569

**Applicant(s)**

RIJPKEMA, EDWIN

**Examiner**

DANIEL MITCHELL

**Art Unit**

2619

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 8/18/2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF/ICE)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Response to Arguments*

**Argument of Claims 1-10:** Applicant's arguments filed 6/18/2008 have been fully considered but they are not persuasive. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

**Arguments of Claims 1-10:** In response to applicant's argument that the Office Action fails to provide motivation for the proposed combination. Motivation was provided for the combination of the Kilkki et al. (U.S. Patent No. 6,411,617 B1) and (Chao et al. - U.S. Patent No. 6,667,984 B1), in **col. 7 lines 24-37** of the Chao reference which teaches that contention resolution is **one** of the basic functions of an ATM switch, not the only function of the switch. Therefore proper motivation was provided to combine the references of Kilkki and Chao.

**Arguments of Claims 1-10:** In response to applicant's argument that the references teach away from the modification, it is noted that the Kilkki reference addresses the

issue of node congestion **Kilki col. 3 lines 45-53** but not output port contention.

Applicant is invited to provide prior citations which show the teaching away of the modification of addressing port contention.

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-10, 12-14, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kilki et al. (U.S. Patent No. 6,411,617 B1), hereinafter referred as Kilki in view of Cisneros (U.S. Patent No. 5,157,654), hereinafter referred as Cisneros.

Regarding claim 1, Kilki disclose a communication network **fig. 8** (**element 110, 112, and 114** teaches an ATM network) comprising one or more interconnected data switches (**element 112 –ATM switch and element 110 - ATM extender** teaches interconnected data switches), each of the interconnected data switches having I/O ports (**elements 116, 117 and elements 122, 123** teaches I/O ports and at least one virtual port (**elements 118 and 120** teaches virtual ports).

However Kilki does not expressly disclose characterized in that the communication network subjecting-said I/O ports and said at least one

**virtual port to one contention resolution process common to the I/O ports and the at least one virtual port.**

Hellwig discloses in **fig. 4 and col. 5 lines 49- 67** teaches virtual ports between the interface ports and the resource, and the physical ports with the switching matrix with a single contention resolution module connected to all ports.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Kilkki to include a single contention resolution process for physical and virtual ports of a switch. One would be motivated as such in order ensure high speed transmission within a switch – **Hellwig col. 5 lines66-67 and col. 6 lines 1-2.**

Regarding claim 2, Kilkki discloses (**fig. 8 element 120** teaches virtual input ports and **element 118** teaches virtual output ports) least one virtual port is a virtual input port or a virtual output port. **Col. 13 lines 23-41** teach elements 118 and 120 are dedicated ports, which are virtual ports, for an external resource).

Regarding claim 3, see similar rejection as claim 2.

Regarding claim 4, Kilkki discloses **col. 13 lines 43-55** (teaches that a virtual port has an identifier) wherein the at least one virtual port is an addressable virtual port.

Regarding claim 5, Kilkki discloses **fig. 8** wherein the at least one virtual port **element 118 and 120** is coupled to at least one resource **element 110**. Also lines 23-41 teaches that SIME extender resource element 110 is coupled to the ATM switch element 112 by virtual ports.

Regarding claim 6, Kilkki discloses **fig. 8** wherein the at least one resource **element 110** (teaches that the resource is external to ATM switch 112) is an external resource.

Regarding claim 7, Kilkki discloses **col. 13 lines 23-26** (teaches the external resource element 110 has the function of configuring ATM cells to SIMA principles), wherein the at least one resource comprises means for configuring.

Regarding claim 8, Kilkki discloses **fig. 8 elements 110 and 112** (teaches the association of the two elements) and **col. 13 lines 23-41**(teaches the external resource is associated with the ATM switch), wherein the at least one resource are means for one of the associated data switches.

Regarding claim 9, see similar rejection as claim 1.

Regarding claim 10, see similar rejection as claim 1.

Regarding claim 12, Kilkki discloses **fig. 8** wherein the at least one virtual port **elements 118 and 120** (teaches a virtual port) is an external port and the at least one virtual port is coupled to an external resource **element 110 SIMA extender** (teaches and external resource that is couple to **element 112 ATM Switch**) that performs a

function associated to the data switch, the function **col. 13 lines 23-41** (teaches that data is multiplexed for the ATM Switch) configuring of the data switch.

Regarding claim 13, Kilkki discloses **col. 13 lines 43-55** (teaches that a virtual port has an identifier) wherein the at least one virtual port is an addressable virtual port.

Regarding claim 14, Kilkki teaches a data switch as to the parent claim. **However Kilkki does not expressly disclose wherein the one contention resolution process treats contention at the at least one virtual port as contention on one of the I/O ports.**

Hellwig discloses in **fig. 4 and lines 49-67** both physical and virtual ports. He also discloses one contention resolution module to address the contention resolution at all ports.

See similar motivation as claim 1.

Regarding claim 16, see similar rejection as claim 14.

Regarding claim 18, see similar rejection as claim 14.

3. Claims 11, 15, 17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kilkki and Hellwig in further view of Cisneros (U.S. Patent No. 5,157,654) hereinafter referred as Cisneros.

Regarding claim 11, Kilkki and Hellwig teach the data switch as to the parent claim. **However Kilkki does not expressly disclose further comprising an internal resource that performs a function associated to the data switch, the function including at least one of testing, debugging, programming and configuring of the data switch, wherein the at least one virtual port is an**

**internal port and the at least one virtual port is coupled to the internal resource.**

Cisneros discloses **col. 12 lines 56-68** an internal switch control module which performs essential control, test and administration of a switch through a dedicated interface which is coupled to the switch port.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Kilkki to include solving contention at an output port. One would be motivated as such in order execute fast contention resolution in a switch architecture that is compact **col. 8 lines 65-68**.

Regarding claim 15, Kilkki discloses a data switch as to the parent claim. **However Kilkki does not expressly disclose wherein Cisneros col. 14 lines 5-11 the one contention resolution process resolves contention resulting from an output port of the I/O ports being addressed by two or more input ports of the I/O ports and the one contention resolution process resolves contention resulting from the at least one virtual port being addressed by two or more input ports of the I/O ports.**

Hellwig discloses in **fig. 4 and lines 49-67** both physical and virtual ports. He also discloses one contention resolution module to address the contention resolution at all ports.

**Cisneros discloses in col. 14 lines 5-11, a contention resolution unit that solves contention when two inputs address a single output port.**



See similar motivation as claim 11.

Regarding claim 17, see similar rejection as claim 15.

Regarding claim 19, see similar rejection as claim 15.

### ***Conclusion***

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **DANIEL MITCHELL** whose telephone number is (571)270-5307. The examiner can normally be reached on Monday - Friday 8:00 am - 5:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shah G. Chirag can be reached on 571-272-3144. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. M./  
Examiner, Art Unit 2619

/Chirag G. Shah/  
Supervisory Patent Examiner, Art Unit 2619